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Atomic Layer Deposition of Dielectrics on Graphene Using Reversibly Physisorbed Ozone

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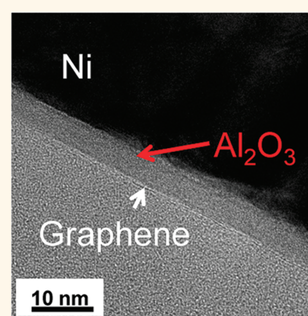
ABSTRACT Integration of graphene field-effect transistors (GFETs) requires the ability to grow or deposit high-quality, ultrathin dielectric insulators on graphene to modulate the channel potential. Here, we study a novel and facile approach based on atomic layer deposition through ozone functionalization to deposit high-κ dielectrics (such as Al_2O_3) without breaking vacuum. The underlying mechanisms of functionalization have been studied theoretically using *ab initio* calculations and experimentally using *in situ* monitoring of transport properties. It is found that ozone molecules are physisorbed on the surface of graphene, which act as nucleation sites for dielectric deposition. The physisorbed ozone molecules eventually react with the metal precursor, trimethylaluminum to form Al_2O_3. Additionally, we successfully demonstrate the performance of dual-gated GFETs with Al_2O_3 of sub-5 nm physical thickness as a gate dielectric. Back-gated GFETs with mobilities of ~19 000 $cm^2/(V\cdot s)$ are also achieved *after* Al_2O_3 deposition. These results indicate that ozone functionalization is a promising pathway to achieve scaled gate dielectrics on graphene without leaving a residual nucleation layer.



KEYWORDS: graphene · dielectrics · atomic layer deposition · noncovalent functionalization · physisorption · nanoelectronics

Graphene has generated a significant interest in the scientific community because of its intriguing electronic,[1−6] optical,[6,7] thermal,[8] and mechanical[9] properties. Graphene, being a truly two-dimensional material with high saturation velocity and long mean free length, makes it an interesting candidate as an alternative material for post-silicon electronics.[5,10−12] A number of novel logic devices using graphene have been proposed for beyond CMOS nanoelectronics.[4,12−14] However, there are several technological hurdles to be overcome in order to realize graphene-based devices in practical applications including growth of conformal, ultrathin, high-quality dielectrics on graphene.[12,15] The ability to precisely control thickness and conformally deposit materials makes atomic layer deposition (ALD) an ideal technique for achieving such dielectrics.[16] However, ALD is a surface-reaction-limited process and graphene, being sp^2-bonded, has no out-of-plane covalent functional groups to initiate the ALD reaction,[16] and scaled high-quality dielectrics down to a few nanometers have not been reported yet. In order to overcome this difficulty, ALD dielectrics have been deposited after different surface preparation techniques such as chemical "functionalization" of graphene *via* nitrogen dioxide (NO_2),[17,18] deposition of a thin metal layer such as Al followed by oxidation[19] or direct deposition of oxide seed layers such as SiO_2, Al_2O_3, or HfO_2,[20] polymer coating,[21,22] and application of organic self-assembled monolayers (SAMs)[23,24] on graphene as nucleation layers. Some of these approaches leave an undesirable seed layer, which might result in the inability to scale the dielectric thickness, or are incompatible with existing silicon technology. Other techniques that are not sensitive to the surface chemistry have also been explored for direct deposition of dielectrics including physical vapor deposition (PVD),[20,25−28] plasma-enhanced chemical vapor deposition (PECVD),[29,30] and plasma-assisted atomic layer deposition (P-ALD).[31] The hostile environments used in these approaches, however, can lead to unintentional doping and/or cause damage to graphene.[15,29,31,32] Direct deposition of HfO_2 on graphene using a low-temperature ALD process has

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been reported.[33,34] However, the mechanism of deposition is not well understood, and only films thicker than 10 nm are continuous.[34] Another interesting approach which has been reported is the physical assembly of dielectric nanostructures such as Al_2O_3 nanoribbons on top of graphene.[35,36] Even though this technique provides good-quality dielectrics, it is not viable for large-scale production. Above all, there are only a few reports regarding aggressive scaling of dielectric thicknesses, possibly due to the difficulty in achieving pinhole-free, thin dielectrics over a large area.

We have previously reported that the use of ozone (O_3) allows for conformal deposition of high-quality ALD Al_2O_3 on graphene without mobility degradation, and top-gate devices with a mobility of 5000 $cm^2/(V \cdot s)$ at room temperature are routinely realized.[37] It was found, however, that the O_3 process at room temperature (~300 K) shows no detectable increase in defect density, whereas a 473 K O_3 process causes significant damage to graphene as verified by *ex situ* Raman measurements.[37] The mechanism of the O_3 adsorption and resultant functionalization of the graphene surface remains unclear. It is critical to understand the effects of O_3 functionalization on graphene in order to be able to extensively apply this process to the deposition of various dielectrics and to successfully scale their thicknesses to a few nanometers. In this work, we investigate the effects of the ozone-based ALD process on the transport properties of graphene using both theoretical and experimental techniques. First, we study the electronic properties of graphene using *ab initio* calculations with respect to physisorption and chemisorption of O_3 and address how they are affected by different adsorption mechanisms. The effects of O_3 adsorption on electrical characteristics of graphene are also investigated experimentally using *in situ* transport measurements of graphene devices exposed to O_3. In order to also get a better understanding of the ALD process, *in situ* transport measurements were also carried out in an ALD reactor using both O_3 and trimethylaluminum (TMA). We then demonstrate high-quality Al_2O_3 growth on graphene with a physical thickness in the sub-5 nm regime with no residual seed layer. The effects of the ALD process on the properties of graphene are discussed based on the extracted mobilities of back-gated GFETs and Raman measurements. The electrical characteristics of dual-gated graphene field-effect transistors (GFETs) fabricated using this approach are also presented.

RESULTS AND DISCUSSION

Physisorption *versus* Chemisorption of O_3: *Ab Initio* Calculations. The electronic properties of the graphene–adsorbate (O_3) systems are studied theoretically using the *ab initio* density functional theory method.

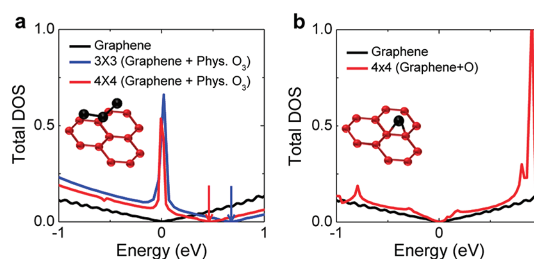

Figure 1. (a) Density of states (DOS) of graphene containing a physisorbed O_3 molecule in 3 × 3 and 4 × 4 supercells. The dominant peaks at 0 eV correspond to that of the O_3 molecules adsorbed on the graphene surface. (b) DOS for the O_3 chemisorption state on graphene (C–O–C) in a 4 × 4 supercell. The energy of the Dirac point of pristine graphene is defined as E_D = 0. Insets in the figures are the schematics of the physisorbed and chemisorbed O_3 molecule on graphene.

Figure 1a,b show the density of states (DOS) as a function of energy (E) for pristine graphene and graphene with O_3 physisorbed and chemisorbed in 3 × 3 and 4 × 4 supercells, respectively. The insets in Figure 1a,b show schematically the physisorption and chemisorption states of O_3 on graphene. Here, "physisorption" is the case where, under equilibrium conditions, the O_3 molecule is in close vicinity of graphene and is *noncovalently* interacting with graphene. The equilibrium distance (or the separation distance) between the physisorbed O_3 molecule and graphene plane is 0.28 nm, and the binding energy for this state is 250 meV,[38] which is much higher than the van der Waals' interactions (~10–100 meV) because of the partial charge transfer from graphene to O_3. In the case of chemisorption, the O_3 molecules chemically react with graphene, resulting in surface-bound carbon–oxygen functional groups such as epoxide (C–O–C), carbonyl (C=O), and carboxyl (O–C=O) groups as well as free gas phase molecules such as O_2, CO, or CO_2.[38–40] Since a chemical (covalent) bond is formed, this state has a higher binding energy of 0.33 eV and a smaller C–O bonding distance of 0.144 nm.[38] It was reported that the energy barrier for epoxide formation from an ozone molecule is 0.74 eV, and the rate of epoxide formation is higher at higher temperatures.[38] In previous XPS studies, it was reported that, when Al_2O_3 is deposited on graphite pretreated with O_3 at 200 °C (473 K), functional groups such as epoxide, carbonyl, and carboxylic groups are present on the graphite surface,[40] and these functional groups eventually cause damage by etching the graphite surface.[38]

In Figure 1a,b, the black curve represents the linear density of states (DOS), a signature of intrinsic single-layer graphene without any interaction with ozone, where the Dirac point is located at 0 (E_D = 0 eV = E_F, Fermi level).[5] The blue and red curves represent the DOS of graphene with a physisorbed/chemisorbed O_3 molecule. The DOS results suggest that physisorbed O_3

on graphene acts as a strong acceptor, which leads to a shift in the Dirac point. It is found that the Dirac point is shifted to 0.7 and 0.5 eV in 3 × 3 and 4 × 4 supercells, respectively (indicated by blue and red arrows). This indicates that physisorbed O_3 on graphene results in p-type doping. The dependence of the shift in the Dirac point on the supercell size is attributed to a different fractional coverage of adsorbed O_3 on graphene. The DOS study also suggests that the physisorbed O_3 does not alter the band structure as the linear dispersion of DOS is maintained, as shown in Figure 1a. The molecular orbitals of O_3 correspond to flat bands and manifest themselves as peaks in the DOS (see Figure 1a). However, chemisorbed O_3 (*e.g.*, an epoxide) on graphene alters its band structure, which results in distortion of the linear dispersion relation, as shown in Figure 1b. In addition, there is no shift in the Dirac point suggesting that the chemisorbed O_3 does not chemically dope the graphene layer. Since an epoxide group is formed by joining two adjacent carbon atoms with an oxygen atom through single bonds, the carbon atoms need to undergo configurational changes from a planar sp^2-hybridization to a distorted sp^3-hybridized structure; that is, it introduces defects in graphene.[41]

One can expect from the DOS study that physisorbed O_3, which chemically dopes graphene, acts as a charged impurity (Coulomb) scatterer, whereas chemisorbed O_3, which results in point or line defects such as an epoxide, acts as short-range (defect) scatterer. It has been theoretically predicted[42−44] and experimentally verified[45,46] that charged impurity scattering (1) decreases the carrier mobility with an increase in impurity concentration (n_{imp}), (2) shifts the gate voltage of minimum conductivity (V_{Dirac}) to positive or negative voltage depending on the type of charged impurity, and (3) broadens the width of the minimum conductivity region, while defect scattering (1) decreases the carrier mobility with an increase in defects (n_d), (2) does not change the residual charge density, and (3) reduces the conductivity at V_{Dirac}.

***In Situ* Transport Measurements: Effects of O_3 Adsorption.** The effects of O_3 on charge transport properties of graphene were investigated *in situ* using back-gated GFETs by exposing the graphene surface to O_3. Figure 2a shows the drain−current (I_{DS}) *versus* back-gate bias (V_{BG}) curves before and after O_3 exposure of a graphene device. In Figure 2a, the black line represents the conductivity curve for the pristine sample measured in vacuum (~6 × 10^{-5} Torr) and shows a V_{Dirac} = +4 V, indicating some amount of unintentional doping in the as-prepared graphene device. It is found that immediately after exposing the device to O_3 for 0.1 s ($p[O_3]$ ~ 0.75 Torr), V_{Dirac} shifts to a more positive voltage (from +4 to +22 V), and as a result, the extracted mobility decreases from 5900 to 3300 $cm^2/(V \cdot s)$ for electrons and from 6600 to 4500 $cm^2/(V \cdot s)$ for holes. After prolonged pumping, V_{Dirac} and mobility values of the graphene device return close to the initial values, as shown in Figure 2a−c, consistent with a physisorbed effect. The mobility values for charge carriers in graphene have been extracted using the model presented by Kim *et al.*[19] and individually fitting the electron and hole branches.[28,29] Comparison of this method with other mobility extraction and measurement methods indicates that the extracted mobility values are quite comparable.[47] This observation indicates that O_3 is physisorbed on graphene at 300 K and acts as an acceptor-type (charged) impurity, thereby attracting electrons from graphene (and thus inducing holes) leading to increased charged scattering and a concomitant decrease in mobility. In order to confirm these results, the same experiment was repeated on three different samples, and the trend observed was similar. Also, further evidence of this can be found in experiments with varying O_3 partial pressure (see Supporting Information), where it is found that there is a positive shift in V_{Dirac} and a drop in the carrier mobility with increasing O_3 partial pressure (*i.e.*, exposure dose). According to the DOS analysis shown in Figure 1, where the physisorbed O_3 on graphene causes a shift in the Dirac point (E_D), while the chemisorbed O_3 alters the band structure of graphene without moving the E_D level, O_3 is likely principally physisorbed on graphene at 300 K.

***In Situ* Electrical Monitoring of the ALD Process.** The above results suggest that O_3 can functionalize graphene through a physisorption process and can provide reactive nucleation sites for subsequent ALD dielectric deposition. This is in good agreement with previous reports where an Al_2O_3 layer using TMA/O_3 could be deposited on graphene.[37] Al_2O_3 deposited using such a process results in conformal deposition and a small change in V_{Dirac} with no detectable increase in defect-induced D band (not shown). However, since we also observed above that physisorbed O_3 leads to a large shift in V_{Dirac}, we performed *in situ* transport measurements of back-gated GFETs in a commercial ALD reactor (see Figure S2 in Supporting Information for details on experimental setup). It is frequently mentioned in the literature that the TMA/H_2O ALD process does not result in deposition of dielectrics on (clean) graphene surfaces,[23] which suggests that TMA does not physisorb *via* charge sharing on the graphene surface like O_3. So, in this study, we assume that TMA by itself would not affect the transport characteristics of graphene and start with an O_3 pulse. Figure 3a presents the conductivity *versus* gate bias curves for *in situ* O_3 and TMA exposures on graphene devices at 300 K. Similar to previous experiments, after ozone exposure ($p[O_3]$ ~ 1 Torr), a positive shift in V_{Dirac} and a drop in the extracted mobility from 2600 to 1150 $cm^2/(V \cdot s)$ for electrons and from 1800 to 1000 $cm^2/(V \cdot s)$ for holes are observed. The shift is smaller in this case because a

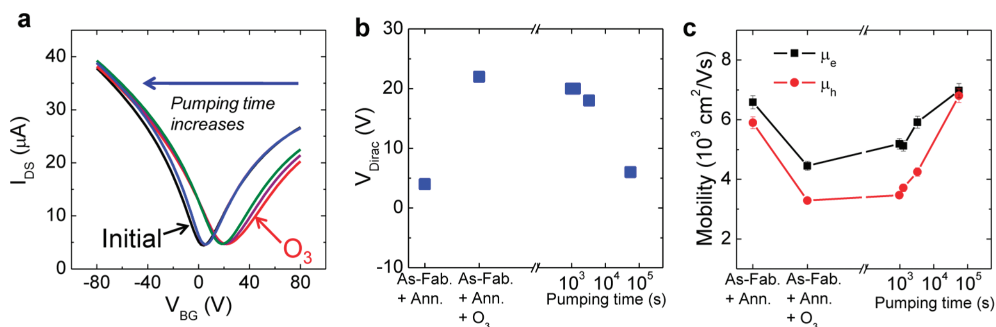

Figure 2. *In situ* transport measurements of a graphene device with O_3 exposures. (a) Drain current (I_{DS}) *versus* back-gate voltage (V_{BG}) curves for a pristine graphene sample (black line), 0.1 s O_3 exposure (red line), and the subsequent measurements with respect to pumping time. (b) Dirac voltage (V_{Dirac}) shifts and (c) electron and hole mobilities as a function of pumping time after O_3 exposure. The error bars represent the variation in extracted mobilities because of the difference in the width of the graphene flake across the channel length.

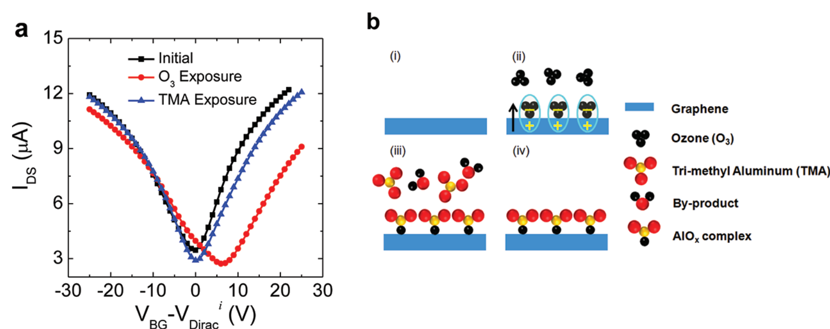

Figure 3. (a) *In situ* transport measurements of a graphene device with O_3 and TMA exposures; drain–current (I_{DS}) *versus* effective gate voltage ($V_{BG} - V_{Dirac}{}^i$, where $V_{Dirac}{}^i$ is the initial Dirac voltage for graphene device before O_3/TMA exposures) curves for pristine graphene sample (black line), after 100 s of O_3 exposure (red line) and after (4 × 0.3 s) TMA exposure. (b) Schematic showing the sequence of ALD reaction: (i) pristine graphene with minimal (ideally zero) residual impurity; (ii) nucleation of graphene surface with O_3 resulting in charge sharing with graphene (graphene is p-doped); (iii) TMA molecule reacts with O_3 physisorbed on graphene surface, resulting in charge neutralization in graphene; (iv) rejuvenated graphene with no additional residual charges with seed layer for subsequent ALD deposition (please note that the schematic shows a simplified representation of molecules such as TMA, which in reality exists as a dimer and is cleaved upon reaction).

thinner back-gate oxide was used in this experiment (ΔV_{Dirac} = 6 V on 90 nm SiO_2 is equivalent to $\Delta V_{Dirac} \cong$ 20 V on 300 nm SiO_2) and could also be due to differences in the chamber types and setup. By subsequent exposure to TMA, the effect from O_3 seems to have been nullified and the V_{Dirac} and mobility values return close to that of initial values. This indicates that, when physisorbed O_3 on graphene reacts with an incident TMA molecule, the O_3 releases the electrons attracted from graphene and participates in the formation of an Al_2O_3 layer. This suggests that the O_3 functionalization scheme can be used for ALD dielectric deposition on graphene without leaving behind any residual seed layer as well as resulting in no net charge transfer to graphene (see schematic shown in Figure 3b).

Scaling Down Al_2O_3 Dielectric Thickness. In order to scale down the dielectric thickness, minimizing the seed layer is important. So, unlike previous studies,[37] where repeated O_3 functionalization was adopted for depositing an Al_2O_3 seed layer, here O_3 functionalization was performed only once at high pressure to increase the number of reaction sites, which was followed by a TMA/H_2O ALD process[16] for Al_2O_3 deposition. Using this approach, a process was developed for depositing thin Al_2O_3 (≤5 nm) on graphene (see Methods section for details regarding Al_2O_3 deposition).

Figure 4a presents the Raman spectrum of single-layer graphene before and after the ALD process, where it is clear that there is no huge increase in D band (1340 cm^{-1}) intensity, suggesting that the dielectric process does not have any significant impact on the graphene properties. We also monitored the effect of the dielectric process on back-gate GFETs by calculating the carrier mobilities before and after deposition of an Al_2O_3 layer with various thicknesses (~4–7 nm). Figure 4b shows the experimental curves of resistance (*R*) *versus* back-gate voltage ($V_{BG}-V_{BG,Dirac}$) of a particular GFET. It is observed that there is a significant increase in carrier mobility *after* dielectric deposition. Several devices were studied to confirm the observed phenomenon (Figure 4c). Although the initial back-gate mobilities vary from ~2600 to 9200 cm^2/(V·s) (all of the mobilities mentioned in this

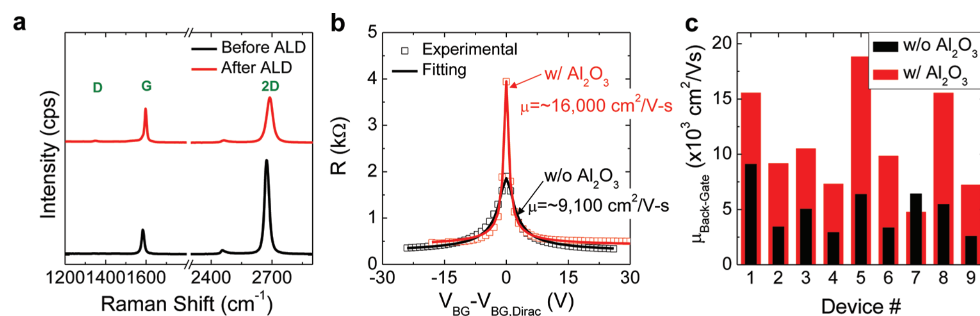

Figure 4. Effect of O_3-based ALD Al_2O_3 on properties of graphene. (a) Raman spectra of single-layer graphene before (black line) and after ALD process (red line). (b) Resistance (R) *versus* back-gate bias ($V_{BG}-V_{BG,Dirac}$) before (black data set) and after ALD process (red data set); electrical measurements (open squares) and model fitting (solid line) for mobility calculations. (c) Comparison of back-gate GFET mobilities before (black bars) and after ALD Al_2O_3 deposition (red bars). Raman and electrical measurements were taken at room temperature (~300 K) and in ambient air. The channel dimensions of the back-gate GFETs shown in these data have varying lengths and widths: length = ~3–15 μm, width = 2–9 μm.

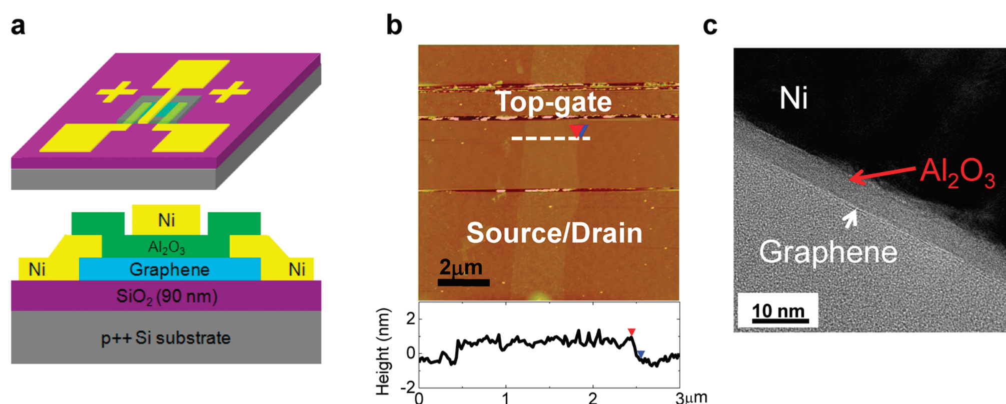

Figure 5. Physical analysis of graphene devices with ALD Al_2O_3 as top-gate dielectric. (a) Schematics showing perspective and cross-sectional views of a dual-gated graphene device. (b) AFM image of top-gated graphene device with O_3-based ALD Al_2O_3. The plot below shows the line profile along the white line showing a smooth surface and a step height (~1.2 nm). (c) Cross-sectional HRTEM image of graphene device confirming a pinhole-free dielectric with a thickness (t_{ox}) of 4.5 ± 0.3 nm.

section are the average of electron and hole mobilities, and the difference between them is less than 30%), the devices show a similar trend of an increase in mobility after dielectric deposition. A maximum back-gate mobility of ~19 000 cm^2/(V·s) is obtained after Al_2O_3 deposition.

The observed increase in mobility could be a contribution from three different phenomena: (1) Al_2O_3 can act as a passivation layer[48] and can prevent diffusion of species such as H_2O and O_2 to the graphene/substrate interface which degrade the carrier mobility in graphene.[49,50] (2) High dielectric constant materials screen out charged impurities acting as long-range Coulomb scatterers and can therefore help enhance the mobility in graphene devices.[51,52] (3) Ozone cleaning of the graphene surface is one of the other possibilities. Graphite/graphene surfaces exposed to air tend to adsorb atmospheric impurities,[53] and also, the lithography process can leave an e-beam resist such as poly(methyl methacrylate) (PMMA) residues, which act as charge scatterers, thereby lowering the carrier mobility in graphene. It has been observed that ozone exposure (~10^6–10^8 L) cleans the graphite/graphene surfaces of these impurities (Wallace, R. M.; *et al.* unpublished data) and therefore could result in an increased mobility.[54] It is noted that the cleaning of the graphene surface is also possible to some extent with the predielectric deposition annealing performed inside the ALD chamber.[54,55]

Figure 5 shows the structural analysis of a dual-gated graphene device with 4.5 ± 0.3 nm Al_2O_3 as top-gate dielectric. The atomic force microscopy (AFM) and cross-sectional high-resolution transmission electron microscopy (HRTEM) analysis of the devices confirm conformal and pinhole-free deposition of the dielectric of thickness over a couple of micrometers with no significant addition to roughness of graphene on SiO_2 (Figure 5b,c and Figure S4 of Supporting Information). The cross-sectional TEM analysis of the devices also confirms the absence of any additional interfacial layer between the graphene and Al_2O_3 layer (note

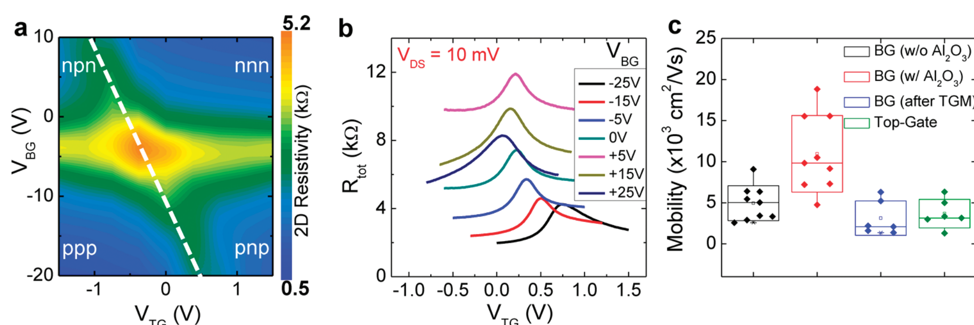

Figure 6. Electrical characteristics of dual-gated GFETs with ALD Al_2O_3 as top-gate dielectric and 90 nm SiO_2 as back-gate dielectric (measured at ~300 K and in ambient air). (a) Two-dimensional resistance (R_{tot}) plot as a function of top-gate voltage (V_{TG}) and back-gate voltage (V_{BG}) for a GFET with 7 nm Al_2O_3. The plot shows the heterojunction. (b) Resistance (R_{tot}) *versus* V_{TG} curves at different V_{BG} for a GFET with 4.5 nm Al_2O_3. (c) Comparison of mobilities of back-gate GFETs as-prepared (black data points), after Al_2O_3 deposition (red data points), after top-gate metallization (blue data points), and completed top-gate GFETs (green data points). The symbols (diamonds) represent individual data points for different devices, and the boxes represent the standard deviation connected by lines to the minimum and maximum values. The abbreviations BG and TGM in the legends of Figure 4c are for back-gate and top-gate metal. The channel dimensions of the top-gate GFETs shown in these data have varying lengths and widths, length = ~0.5−2 μm, width = 2−9 μm, while back-gate dimensions are the same as that mentioned for Figure 4.

the uniformity in color contrast of the top dielectric layer in Figure S4 of Supporting Information).

Figure 6 shows the electrical characteristics of the dual-gated graphene devices with various thicknesses (4−7 nm) of ALD Al_2O_3 as top-gate dielectric. Figure 6a shows the two-dimensional (2D) resistance plot of a GFET with a 7 nm Al_2O_3 top-gate dielectric. The 2D plot presents the combined effect of back-gate voltage (V_{BG}) and top-gate voltage (V_{TG}) on the measured resistance, and it clearly shows the heterojunction behavior in a partially covered GFET.[37] Figure 6b shows the two-terminal resistance plot of a GFET (with 4.5 nm Al_2O_3) as a function of V_{TG} at various back-gate biases ($V_{BG} = -25$ to $+25$ V) and at a drain bias (V_{DS}) of 10 mV. The slope of the Dirac voltage for top-gate ($V_{Dirac,TG}$) and back-gate voltage (V_{BG}) curve (white dashed line in Figure 6a) gives a coupling constant between top-gate and back-gate oxides. Using the following equation, $(C_{TG}/C_{BG}) = -(1/\text{slope})$, where C_{TG} and C_{BG} are the top-gate and back-gate capacitances (0.0383 μF/cm^2 for a SiO_2 layer with a thickness of 90 nm and relative dielectric constant of 3.9), the C_{TG} is obtained. The slope of the $1/C_{TG}$ *versus* dielectric thickness (t_{ox}) is used for extracting the dielectric constant of Al_2O_3 (not shown) and is found to be ~7.3, which is a reasonable value for ALD Al_2O_3 deposited at 423 K.[56] Figure 6c shows the comparison of the mobilities extracted for back-gate GFETs as-prepared, after Al_2O_3 deposition (different thicknesses ~4−7 nm), after top metal gate fabrication and top-gate GFETs.[19,28,29] It is found that the O_3-based ALD process for depositing high-κ dielectrics does not cause any mobility degradation in graphene as reported frequently in the literature for other techniques.[12,21,25] On the other hand, the top-gate device mobilities lie in the range of 3000−5000 cm^2/(V·s) (see Figure 6c). It is seen that the mobility of the GFETs degrades after the gate metallization process (60 nm Ni, e-beam evaporated). This is potentially due to the X-ray damage of gate dielectrics resulting in charged defects in the oxide or damage of graphene itself.[57] More detailed studies of the degradation are being investigated. All the top-gate GFETs show a hysteresis of ≤50 mV. The leakage current through the 4.5 nm Al_2O_3 dielectric was below 3×10^{-13} A for an electric field of 2 MV/cm at top-gate with an area of 4.5 μm^2 (not shown). All of the above results are consistent with high-quality, pinhole-free, and thin high-κ dielectrics with large capacitance which provide a good control of the graphene channel and can be obtained using an ozone functionalization based ALD technique.

CONCLUSIONS

In entirety, we have developed an ALD technique using an O_3 functionalization scheme and established the fundamental mechanisms for depositing residual seed-layer-less, high-quality, and thin high-κ dielectrics on graphene in a single reactor. We have investigated and illustrated the effects of O_3 adsorption on graphene using *in situ* electrical characterization and *ab initio* density functional theory calculations with respect to physisorption and chemisorption of O_3. The theoretical study of DOS of graphene−O_3 systems reveals that physisorption of O_3 results in a positive shift in Dirac point (p-doping) while preserving the band structure of graphene, but chemisorption of O_3 leads to defect generation and destruction of the linear dispersion relation of pristine graphene. Therefore, the charge transport in graphene devices is likely to be dominated by charge impurity scattering in the case of physisorption and defect scattering in the case of chemisorption. Our experiments reveal that O_3 interaction with graphene at 300 K results in a reversible p-type doping in graphene, suggesting that O_3 adsorption follows the physisorption process. It is found that the effects of O_3 doping are also reversible upon

subsequent exposure to TMA. This study shows that O_3 functionalization of the graphene surface provides a nondestructive way of nucleating growth for a dielectric layer. We also investigated the effect of the dielectric deposition process on graphene and found that back-gate GFET mobilities increase by almost 2× after Al_2O_3 deposition. We show that the electrical characteristics of dual-gated GFETs with Al_2O_3 (physical thickness of 4.5 nm) as top-gate dielectric can result in high mobility GFET performance.

METHODS

Theoretical Calculations. We have used the Vienna Ab Initio Simulation package (VASP)[58,59] with projector-augmented wave (PAW) pseudopotentials[60,61] within the local spin density approximation.[62] Using a periodic boundary condition, a single O_3 adsorbate is modeled in 3 × 3 and 4 × 4 graphene supercells by using a single-layer graphene model with 1.0 nm vacuum separating periodic image in the vertical direction. The ozone molecule is placed 0.3 nm above the graphene plane for the case of physisorption, and an epoxide is introduced for the chemisorption case following the details given in refs 38 and 41.

Device Fabrication and Measurement Details. Graphene flakes were prepared by mechanical exfoliation of natural graphite and transferred onto thermally grown SiO_2 on a low resistivity (0.005−0.01 Ω·cm), p-type (boron-doped) Si wafer serving as a global back-gate electrode. Raman spectroscopy (Nicolet Almega XR Raman system) and optical microscopy were used to identify the number of graphene layers.[63] Back-gated GFETs were prepared on single-layer graphene using standard electron-beam lithography (EBL) technique to define the source/drain regions, followed by metal evaporation onto graphene using an e-beam evaporation process.

For *in situ* ozone experiments, back-gated GFETs were fabricated using the EBL technique described above with ∼290 nm SiO_2 as back-gate dielectric and a metal stack of Cr/Au (5 nm/50 nm) for contacts. The devices were then transferred to a cryogenic probe station (Lake Shore) for transport measurements. Prior to electrical measurements, the devices were annealed in high-vacuum (∼6×10^{-5} Torr) at 350 K for 3 h and cooled to room temperature (∼300 K) in order to remove adsorbed gas species or residual contaminants from the lithography process. For O_3 exposures of graphene, O_3 gas of ∼380 g/Nm^3 concentration (TMEIC OP-250H-LT ozone gas generating system) was introduced into the chamber. *In situ* transport measurements were also carried out in a modified commercial ALD reactor (Cambridge Nanotech Inc., Savannah 200). For these measurements, back-gated GFETs were fabricated using the EBL technique described above with 90 nm SiO_2 as back-gate dielectric and 60 nm Ni for contacts. The device was then mounted on a Au-coated package for wire bonding the source, drain, and back-gate electrodes in order to make electrical contact with the feed through extensions. All of the electrical measurements were carried out at 300 K using an Agilent HP 4155A semiconductor analyzer.

For dielectric thickness scaling studies, back-gated GFETs were fabricated using the EBL technique described above with ∼90 nm SiO_2 as back-gate dielectric and 60 nm Ni for contacts. Electrical measurements were carried out on the as-prepared back-gate GFETs. The samples were then transferred to a commercial ALD reactor (Cambridge Nanotech Inc., Savannah 200) for dielectric deposition. In order to remove any residual contaminants on the graphene surface from device fabrication process, prior to dielectric deposition, back-gated GFETs were annealed in the ALD chamber at 573 K for 2 h in Ar (p[Ar] ∼ 0.7 Torr, 100 sccm) and cooled to 300 K. The graphene samples were then functionalized with O_3 ($p[O_3]$ ∼ 250 Torr), and then Al_2O_3 was grown using TMA/H_2O (4 cycles at 300 K and 32 cycles at 423 K, yielding a thickness of ∼4.5 nm). In order to obtain high-pressure O_3, first the Ar flow was shut off and then a short pulse (0.1 s) of O_3 was introduced into the ALD chamber with the gate valve closed. This increases the chamber pressure to ∼250 Torr. Ozone was held at this pressure in the chamber for 5 min and then purged with Ar. This was repeated three times to ensure sufficient coverage of physisorbed O_3. For obtaining Al_2O_3 films of different thickness, the number of TMA/H_2O cycles at 423 K was varied. The GFETs were electrically characterized again following Al_2O_3 deposition. The top-gate region was defined using EBL, followed by e-beam evaporation of 60 nm Ni as top-gate metal. All of the Ni depositions were started slowly with a deposition rate of 0.1 Å/s and then gradually increased to 0.5 Å/s within the first 20 nm Ni deposition. This is done in order to have good adhesion of the metal to graphene or oxide. The dual-gated devices were then further electrically characterized. All of the electrical measurements in this study were carried out at room temperature and in ambient air using a Cascade probe station and an Agilent HP 4155A semiconductor analyzer.

All of the surface profile data were obtained using a Veeco Dimension 5000 SPM with a Nanoscope Controller V, and the cross-sectional data were obtained using a JEOL JEM-2100 transmission electron microscope (TEM).

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: We provide additional data and information on *in situ* and dielectric thickness scaling experiments including a panoramic TEM picture showing uniform dielectric deposition on graphene using a high-pressure ozone functionalization approach. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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